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Fault Loop Impedance: Principles and Applications

Introduction

Electrical safety begins with the understanding of fault loop impedance. This crucial parameter determines how quickly protective devices respond to faults, preventing electrical shocks, fires, and equipment destruction.

This write-up provides comprehensive guidance on understanding, measuring, and managing fault loop impedance in electrical Installations following the regulatory requirements and standards for ensuring safe and reliable electrical systems.

Industry professionals, designers, installers, and maintenance personnel of electrical installations and students will benefit from the importance of fault loop impedance and its critical role.

1. *Requirement of fault loop impedance measurement*

Fault can occur in an electrical installation between (i) supply conductor and earth or neutral as earth fault or (ii) between supply conductors and between supply conductor and neutral as short circuit. Since such faults can cause thermal effects (fire) or shock (electrocution), automatic disconnection of supply within the specified time is necessary to ensure safety. Protective measures by automatic disconnection of supply, additional protection by the residual current protective device (RCD) are the measures prescribed under cl. 4.2.11 of IS 732. Verification of fault loop impedance can identify the oversized protective devices or undersized conductors for taking correction measures for compliance to ensure safety.

2. *Compliance measures prescribed by the Regulations and Standards*

Compliance with this measure is ensured by conducting a Fault Loop Impedance Test as a verification measure prescribed in the following Regulations and Standards:

i. Regulation 43 of the Central Electricity Authority (Measures relating to Safety and Electric Supply) Regulations, 2023.
ii. Chapter 6 of IS 732: 2019 (Code of Practice for Electrical Wiring Installations)
iii. Clause 6.3.2 of IS 17900: 2022 (Lift and Elevators)
iv. Clause 4.4.4.4 of IS: 14242 (Uninterruptible power system Part 1: Safety requirements)
v. Cl. 23.0.7 to 23.0.9 of IS 3043:2018 (Code of Practice for Earthing)

3. *Fault loop impedance and protection by automatic disconnection*

The maximum allowable fault loop impedance value is related to the disconnection time, the current causing effective operation of the overcurrent protective device (OCPD), and the touch voltage relating to the type of earthing system. Hence, information on the impedance offered by the conductor materials forming the fault loop and the tripping characteristics of the overcurrent protective device is required. The instantaneous trip current value of OCPD relies on the premise that the fault clearance within a duration of 0.4s at a touch voltage of 230V, protects the person (refer Fig. 1).

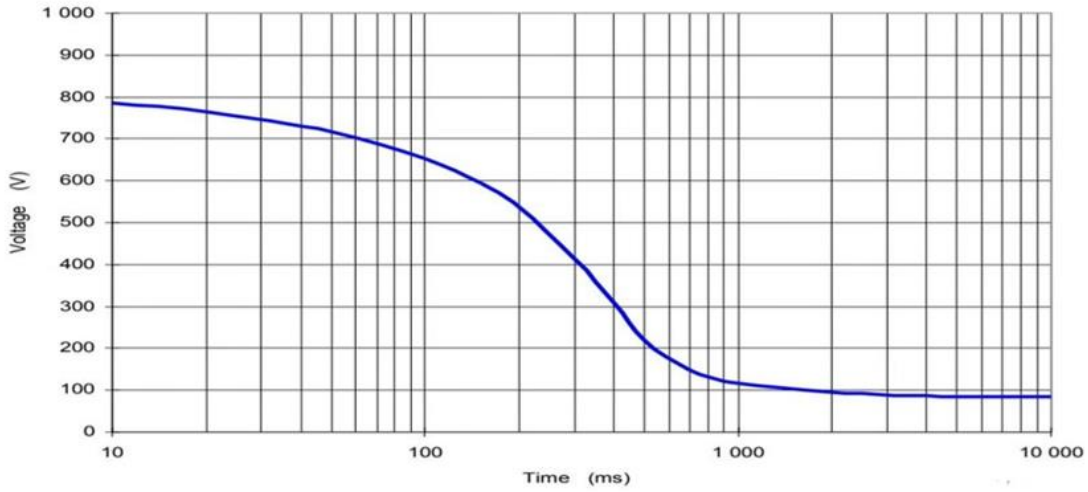


Fig.1: Tolerable touch voltage (UTP), (Fig-28 of IS 732)

Based on the above, typical protection for the final circuit in an LV installation is ensured by fixing the Maximum Disconnection Times as per Table 1 of IS 732 for various touch voltages, in the TN, and TT earthing systems.

System	50 V <*Uo* ≤ 120 V s		120 V <*Uo* ≤ 230 V s		230 V <*Uo* ≤ 400 V s		*Uo* > 400 V s	
	a.c.	d.c.	a.c.	d.c.	a.c.	d.c.	a.c.	d.c.
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)
TN	0.8	Note 1	0.4	5	0.2	0.4	0.1	0.1
TT	0.3	Note 1	0.2	0.4	0.07	0.2	0.04	0.1
Where in TT systems the disconnection is achieved by an overcurrent protective device and the protective equipotential bonding is connected with all extraneous-conductive-parts within the installation, the maximum disconnection times applicable to TN systems may be used. *Uo* is the nominal a.c. or d.c. line to earth voltage.								
NOTES 1 Disconnection may be required for reasons other than protection against electric shock. 2 Where disconnection is provided by an RCD *see* Note to **4.2.11.4.4**, Note 4 to **4.2.11.5.3** and Note to **4.2.11.6.4**.								

Table 1: Maximum Automatic Disconnection Times for Fault Protection by Automatic Disconnection

It can be understood from Table 1 that fault protection through automatic disconnection of overcurrent protective devices, within a specified duration for various line-to-earth voltages of the respective circuits (touch voltages) ensures the safety of persons and property. Hence, the fault loop impedance, applicable touch voltage, and time-current characteristics of the OCPDs are required in the design.

4. Maximum allowable value of Fault Loop Impedance

In the TNS system, the characteristics of the protective devices and the circuit impedances shall fulfill the following requirements as per cl.4.2.11.4.4 of IS 732:

$$Z \leq U_o / Ia \quad \text{..... Expression 1}$$

where Z= the impedance in ohms (Ω) of the fault; Ia = the current in amperes (A) causing the automatic operation of the disconnecting device within the time

specified in 4.2.11.3.2.2 or 4.2.11.3.2.3 and U_o = the line conductor to the earthed neutral voltage, 230V.

The fault loop impedance for a TNS system can be arrived at from the above expression by substituting the value for Ia as found from cl.5 below.

To arrive at the fault loop impedance **Z** in a TT system, the expression in Cl. 4.2.11.5 of IS 732 should be adopted. For the IT Systems, the expression in Cl.4.2.11.6.3 of IS 732 should be adopted.

Where a residual current protective device (RCD) is used for fault protection, the following condition shall be fulfilled:

− RA × I Δn ≤ 50 V as required by 4.2.11.5.3 of IS 732

Where, RA is the sum of the resistance in ohms (Ω) of the earth electrode and the protective conductor for the exposed conductive-parts, IΔn is the rated residual operating current of the RCD.

Notes

i. Fault protection is provided in this case even if the fault impedance is high compared to the TN system.
ii. Where discrimination between RCDs is necessary, see IS 732:5.3.6.3.
iii. The disconnection times following Table 1 relate to prospective residual fault currents significantly higher than the rated residual operating current of the RCD (typically 5 IΔn).

For all the earthing systems, compliance is ensured by conducting a test as per cl.4.2.11.4 and Cl. 6.2.3.6.2 of Annex MM of IS 732.

Since compliance is to be ensured by conducting the Fault Loop Impedance Test and such a test is conducted at the normal operating temperature of the circuit, 2/3rd of the fault loop impedance value as calculated above should be considered due to higher resistance that could result during the fault condition.

The maximum allowable value of the fault loop impedance is ≤ 2/3rd of the calculated fault loop impedance Z (as calculated from Expression 1)……..Expression 2

5. *Characteristics of different types of OCPDs*

A) MCBs up to 125A

While U_o is a constant value found from Expression 1, the magnitude of current should be obtained from the time current characteristics of the OCPDs for arriving at the maximum allowable value of the fault loop impedance. The characteristics of different types of MCBs up to 125A AC can be found in Table 7 of IEC 60898-1 as given in the following Table 2 below:

Test	Type	Test current	Initial condition	Limits of tripping or non-tripping time	Result to be obtained	Remarks
a	B, C, D	1,13 I_n	Cold [a]	$t \leq 1$ h (for $I_n \leq 63$ A) $t \leq 2$ h (for $I_n > 63$ A)	No tripping	
b	B, C, D	1,45 I_n	Immediately following test a	$t < 1$ h (for $I_n \leq 63$ A) $t < 2$ h (for $I_n > 63$ A)	Tripping	Current steadily increased within 5 s
c	B, C, D	2,55 I_n	Cold [a]	1 s < t < 60 s (for $I_n \leq 32$ A) 1 s < t < 120 s (for $I_n > 32$ A)	Tripping	
d	B C D	3 I_n 5 I_n 10 I_n	Cold [a]	$t \leq 0,1$ s	No tripping	Current established by closing an auxiliary switch
e	B C D	5 I_n 10 I_n 20 I_n [b]	Cold [a]	$t < 0,1$ s	Tripping	Current established by closing an auxiliary switch

NOTE An additional test, intermediate between c and d, is under consideration for circuit-breakers of type D.

[a] The term "cold" means without previous loading, at the reference calibration temperature.

[b] 50 I_n for special cases.

Table 2: Tripping Characteristics of AC MCBs

The tripping time of less than 0.1s for an instantaneous tripping of electromagnetic release is prescribed for the B, C, and D type MCBs for a current multiple of 5, 10, and 20 times the rated current of the above MCBs respectively. Based on the characteristics of AC MCBs from the above Table and applying Expressions 1 & 2 above, the fault loop impedance value and the maximum allowable values for the different characteristics of a 6 A, AC MCB are furnished below:

Rating of MCB Amps	Type of MCB	Instantaneous tripping current Amps	Fault loop impedance Ohms	Maximum allowable value of Impedance for validation Ohms
6	B	5*6=30	230/30=7.67	7.67*2/3=5.11
6	C	10*6=60	230/60=3.83	3.83*2/3=2.56
6	D	20*6=120	230/120=1.92	1.92*2/3=1.28

Table 3: Typical calculation of maximum allowable Fault loop impedance values

Similarly, fault loop impedance for DC circuits can be calculated based on the characteristics from Table 7 of IEC 60898-2 furnished in Table 4 below:

Test	Type	Test current a.c.	Test current d.c.	Initial condition	Limits of tripping or non-tripping time	Result to be obtained	Remarks
a	B, C	1,13 I_n		Cold*	$t \geq 1$ h ($I_n \leq 63$ A) $t \geq 2$ h ($I_n > 63$ A)	No tripping	
b	B, C	1,45 I_n		Immediately following test a	$t < 1$ h ($I_n \leq 63$ A) $t < 2$ h ($I_n > 63$ A)	Tripping	Current steadily increased within 5 s
c	B, C	2,55 I_n		Cold*	1 s < t < 60 s ($I_n \leq 32$ A) 1 s < t < 120 s ($I_n > 32$ A)	Tripping	
d	B C	3 I_n 5 I_n	4 I_n 7 I_n	Cold*	0,1 < t < 45 s ($I_n \leq 32$ A) 0,1 < t < 90 s ($I_n > 32$ A) 0,1 < t < 15 s ($I_n \leq 32$ A) 0,1 < t < 30 s ($I_n > 32$ A)	Tripping	Current established by closing an auxiliary switch
e	B C	5 I_n 10 I_n	7 I_n 15 I_n	Cold*	t < 0,1 s	Tripping	Current established by closing an auxiliary switch
* The term "cold" means without previous loading, at the reference calibration temperature.							

Table 4: Tripping Characteristics of DC MCBs

Based on the characteristics of DC MCBs from Table 4 and applying Expressions 1 & 2, the fault loop impedance and the maximum allowable values for the different characteristics of DC MCBs can be calculated. e.g. It requires 7 times rated current for the 6A, B type, DC MCB to achieve an instantaneous trip. So 2/3 of 230/(7*6) = 3.65 Ohms will be the maximum allowable fault loop impedance.

B) Fuses as OCPDs

The time-current characteristics of various fuses as per IEC 60269-1is furnished in Table 5.

1	2	3	4	5
I_n for "gG" I_{ch} for "gM" [b]	I_{min} (10 s) [c]	I_{max} (5 s)	I_{min} (0,1 s)	I_{max} (0,1 s)
A	A	A	A	A
16	33	65	85	150
20	42	85	110	200
25	52	110	150	260
32	75	150	200	350
40	95	190	260	450
50	125	250	350	610
63	160	320	450	820
80	215	425	610	1 100
100	290	580	820	1 450
125	355	715	1 100	1 910
160	460	950	1 450	2 590
200	610	1 250	1 910	3 420
250	750	1 650	2 590	4 500
315	1 050	2 200	3 420	6 000
400	1 420	2 840	4 500	8 060
500	1 780	3 800	6 000	10 600
630	2 200	5 100	8 060	14 140
800	3 060	7 000	10 600	19 000
1 000	4 000	9 500	14 140	24 000
1 250	5 000	13 000	19 000	35 000
[a] Values for fuses with rated current less than 16 A are given in subsequent parts.				
[b] For "gM" fuse-links, see 5.7.1.				
[c] I_{min} (10 s) is the minimum value of current for which the pre-arcing time is not less than 10 s.				

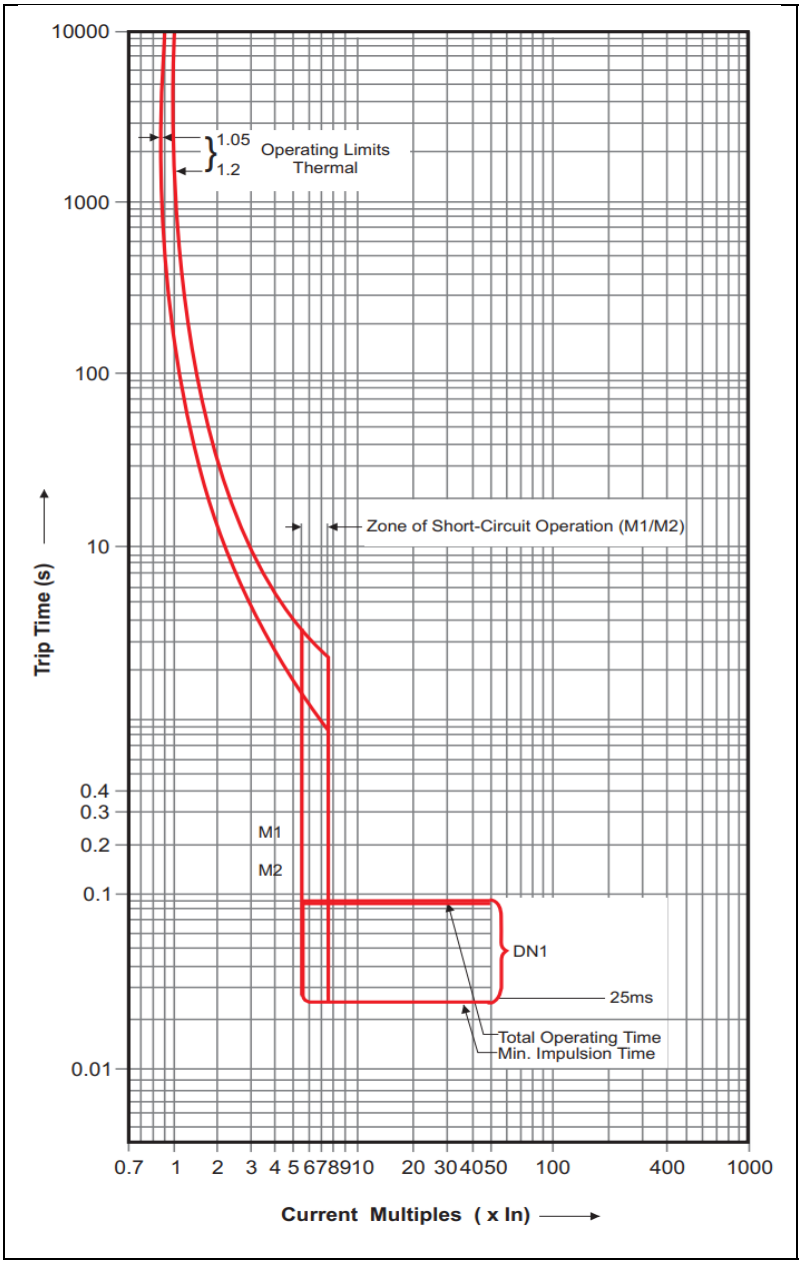
Table 5: Time-current characteristics of HRC fuse

The fault loop impedance and maximum allowable values can be calculated based on the time-current characteristics of HRC Fuse from Table 5 and applying Expressions 1 & 2. e.g. It requires 150 A for the 16A fuse to clear the fault within 0.1s. Hence, 2/3 of 230/(150) = 1.022 Ohms will be the maximum allowable fault loop impedance.

C) OCPDs exceeding 125 A

However, in the case of OCPDs like MCCBs and Circuit Breakers, the tripping current settings provided at such OCPDs should be considered. These OCPDs possess operational

characteristics declared by the manufacturers as per IEC 60947-2. Unlike MCBs, these OCPDs are provided with trip settings for various situations like long time delay for overload, short time delay for overcurrent in the downstream circuits to afford discrimination among the protective gears of the same circuit for supply continuity, and instantaneous tripping whenever the overcurrent value exceeds the settings adopted for the short-time trip. The manufacturer's time-current characteristics curve of an 800A ACB is furnished in Fig.2.



The instantaneous trip occurs when the overcurrent exceeds the value of the short-time trip curve and takes a duration of less than 0.1s. This minimum value of current causing the tripping of the circuit breaker instantaneously to clear the fault is obtained from the settings provided for the breaker. This value is applied in Expression 1 to calculate the required fault loop impedance. In this curve, the instantaneous trip occurs when the pick-up setting of 8 × In i.e. 8 × 800 = 6400A is exceeded.

Based on the characteristics and Expression 1 above, the fault loop impedance value for the 800A, ACB is 230 V/6400 A = 0.0359 Ohm. Applying Expression 2 above, in this case, the maximum allowable value of the fault loop impedance is **0.0359 * 2/3 = 0.0239 Ohm.**

Fig 2: Time-current characteristics curve of an 800A, ACB

A similar approach can be made for the downstream OCPDs from the trip settings as per operational characteristics declared by the manufacturer. From the typical time-current characteristics curve of 160A MCCB given in Fig.3, an instantaneous trip occurs when the pick-up setting of 10 × In i.e. 10 × 160 = 1600A is exceeded. This value has to be considered for calculating the maximum allowable value of the fault loop impedance.

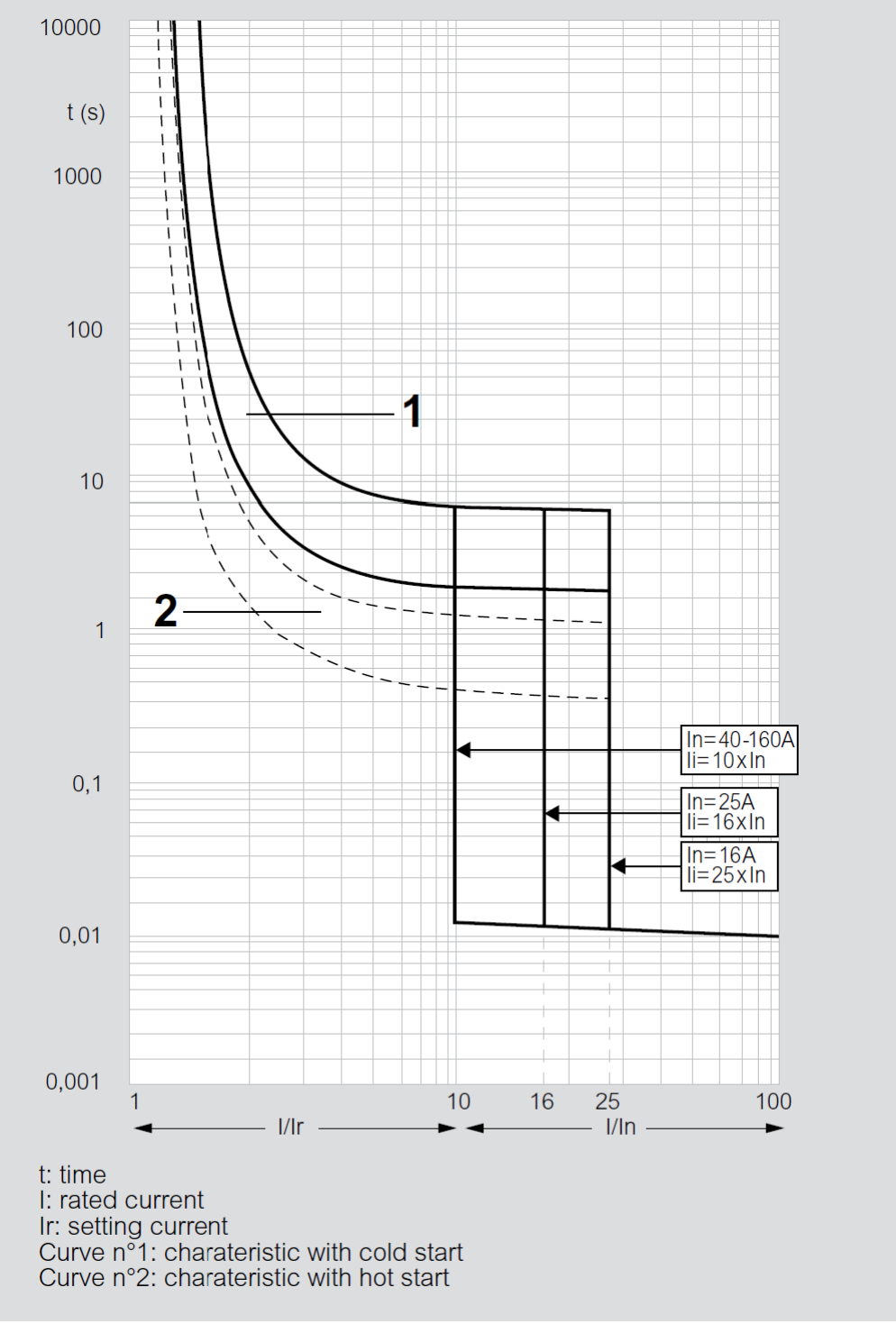


Fig 3: Time-current characteristics curve of 160A MCCB

6. Calculation of fault loop impedance in the existing arrangement

6.1. Fault loop contributing conductors

The impedance of the fault current loop starting and ending at the point of fault is the fault loop Impedance. Typical circuit conductors contributing to the fault loop impedance are shown in Fig.4.

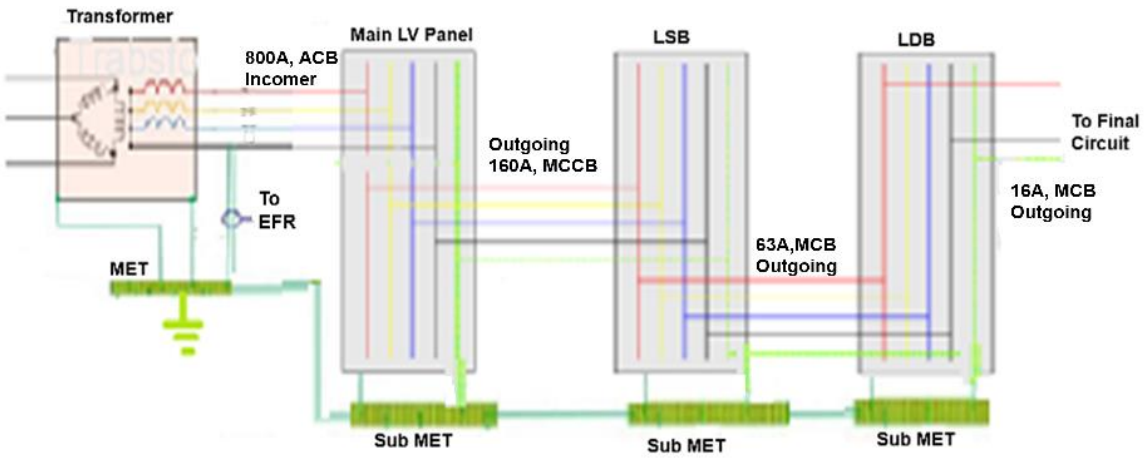


Fig. 4: Fault loop contributing conductors

The earth fault loop comprises the following components:

A) the protective earthing conductor (from the point of fault to the sub-MET);

B) sub-MET to the MET;

C) (i) the earthing conductor from the MET to the neutral terminal of the supply conductor, (ii) from the neutral of the supply conductor up to the source winding, in the case of TN systems (the impedance through earth electrodes need not be considered since it is considerably higher and inconsistent);

or

(iii) the earthing conductor from the MET to the earth electrode provided for the equipment, general mass of earth, (iv) the earthing conductor to the neutral terminal of the supply conductor, the neutral of the supply conductor up to the source winding, in the case of TT and IT systems;

D) the source winding;

E) the line conductor from the supply source like transformer or generator up to the point of fault.

6.1.1 Source impedance

The source impedance can be calculated using the following expression:

Impedance of the source (Refer equation 7 of IEC 60909-0) = % Z* (kV)(kV)/{100*(MVA of the source)}……..Expression 3

where %Z is the percentage impedance, kV is the LV side voltage of the Transformer or the generator, MVA is the apparent rating of the Transformer or the generator.

a. The percentage impedance as per manufacturers' data may be considered for transformers and generators to arrive at the source impedance. However, in the absence of such details during the initial design stage, percentage impedance for the transformers may be considered based on Table 6.

Short-circuit impedance at rated current	
Rated Power kVA	Minimum short circuit impedance %
25 to 630	4
631 to 1250	5
1251 to 2500	6
2501 to 6300	7

Table 6: Recognised minimum value of short circuit impedance for transformers as per Table-1 of IEC 60076-5

b. Regarding generators, 16 % may be considered for % Z during the initial design stage.

6.1.2 Other fault loop contributing conductors

It should be noted that the maximum allowable fault loop impedance offered by different circuit conductors determines the proper selection and trip settings of the OCPDs. The type of material, size, and length of conductors forming the fault loop must be known to calculate fault loop impedance.

The DC resistance of different conductors can be obtained from the relevant Tables of IS 8130 (Refer Table 7 for typical conductors).

Table 2 Stranded Conductors for Single Core and Multicore Cables (Class 2)
(*Clauses* 6.2.3, 6.3.3 *and* 7.3.1)

Sl No.	Nominal Cross-Sectional Area	Minimum Number of Wires in the Conductor				Maximum Resistance of Conductor at 20°C		
		Circular Conductor (Non-Compacted)		Circular Compacted or Shaped Conductor		Copper Conductor		Aluminium Conductor
						Plain Wires	Tinned Wires	
(1)	mm² (2)	Cu (3)	Al (4)	Cu (5)	Al (6)	Ω/km (7)	Ω/km (8)	Ω/km (9)
i)	1	3	—	—	—	18.1	18.2	—
ii)	1.5	3	3	—	—	12.1	12.2	18.1
iii)	2.5	3	3	—	—	7.41	7.56	12.1
iv)	4	7	3	—	—	4.61	4.70	7.41
v)	6	7	3	—	—	3.08	3.11	4.61
vi)	10	7	7	6	—	1.83	1.84	3.08
vii)	16	7	7	6	6	1.15	1.16	1.91
viii)	25	7	7	6	6	0.727	0.734	1.20
ix)	35	7	7	6	6	0.524	0.529	0.868
x)	50	19	19	6	6	0.387	0.391	0.641
xi)	70	19	19	12	12	0.268	0.270	0.443
xii)	95	19	19	15	15	0.193	0.195	0.320
xiii)	120	37	37	18	15	0.153	0.154	0.253
xiv)	150	37	37	18	15	0.124	0.126	0.206
xv)	185	37	37	30	30	0.099 1	0.100	0.164
xvi)	240	61	37	34	30	0.075 4	0.076 2	0.125
xvii)	300	61	61	34	30	0.060 1	0.060 7	0.100
xviii)	400	61	61	53	53	0.047 0	0.047 5	0.077 8
xix)	500	61	61	53	53	0.036 6	0.036 9	0.060 5
xx)	630	91	91	53	53	0.028 3	0.028 6	0.046 9
xxi)	800[1]	91	91	53	53	0.022 1	0.022 4	0.036 7
xxii)	1 000[1]	91	91	53	53	0.017 6	0.017 7	0.029 1
xxiii)	1 200[2]	—	[3]	—	—	0.015 1	0.015 1	0.024 7
xxiv)	1 400[2]	—	[3]	—	—	0.012 9	0.012 9	0.021 2
xxv)	1 600[2]	—	[3]	—	—	0.011 3	0.011 3	0.018 6
xxvi)	1 800[2]	—	[3]	—	—	0.010 1	0.010 1	0.016 5
xxvii)	2 000[2]	—	[3]	—	—	0.009 0	0.009 0	0.014 9
xxviii)	2 500[2]	—	[3]	—	—	0.007 2	0.007 2	0.012 7

[1] These are segmental conductors.
[2] Can be either stranded or segmental.
[3] The minimum number of wires for these sizes is not specified. These sizes may be constructed from 4, 5 or 6 equal segments (Milliken).

NOTE — In case 800 and 1 000 square mm if constructed as per segment construction then the minimum number of wires is not specified. However the number of segments can be 4, 5 or 6.

Table 7: DC Resistance of Copper and Aluminium Conductors

For conductor materials not listed in these tables, the DC resistance can be calculated from the following expression:

R= ᵖ * L/A……..Expression 4

where L is the length in m; A is the cross-sectional area of the conductor in sq.mm; ᵖ is the specific resistance at 20 deg C, Ohm-mm, and R is the DC Resistance at 20 deg C in Ohms. The values of ᵖ for various conductor materials are furnished below as per Table 57 of IS 732, 2019, and from the data provided in IEC 60909-2. Value of Specific Resistivity as per Table 57 of IS 732-2019 are as follows:

Conductor Material	Specific Resistivity ρ at 20°C in Ohm-mm
Copper	17.241*10^-6
Aluminium	28.264*10^-6
Steel	138*10^-6

6.1.3 Challenges and mitigation due to higher impedance of the source and other devices

The FLIT checks whether the OCPD will trip for the measured fault loop impedance. So, the higher loop impedance test values will become a challenge wherever the presence of power electronics equipment like UPS, stabilizer, and isolation transformer introduce higher circuit impedances. The generator's source impedance will generally be 3 to 4 times that of the transformer.

a) As far as UPS is concerned, the earthing arrangement depends on the UPS configuration. If there is an isolation transformer in the UPS circuit, a TNS earthing system should be provided on the secondary of the isolation transformer. In transformer-less UPS, the neutral will be continuous from the upstream and any further separate earth electrode for the UPS will be incorrect. In both cases, the dedicated earth electrode for the UPS is a non-standard practice.

b) OCPDs in such circuits are subjected to a variety of situations. Hence, the coordination scheme for the OCPDs with the combination of transformer and generator sources and interfaces like UPS, isolation transformer, and stabilizer is achieved in the

design as per IEC TS 61200-203 furnished in Fig. 5.

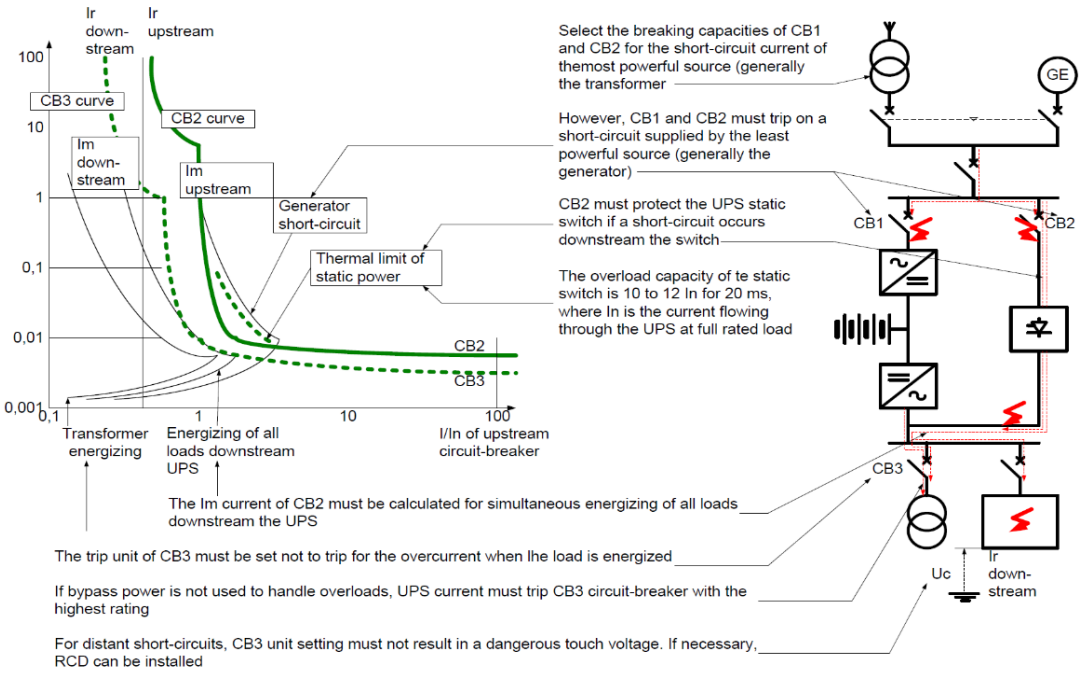


Fig.5: Coordination of OCPDs for a combination of transformer, generator, and UPS circuits to a common load

c) It is hence imperative that compliance of maximum allowable loop Impedance value with the stringent combination of generator, UPS, and isolation transformer will automatically satisfy the maximum allowable loop Impedance value with the transformer source.

d) However, the FLIT for the transformer source should be conducted at the main changeover panel to ensure compliance.

7. *Calculation for the compliance of Maximum allowable earth fault loop impedance for a TNS earthing system in a typical industrial location*

A. Table 8: DATA

Sl. No.	Earth Fault Loop Impedance contributing parameters	Details of the parameters
I	Fault loop impedance seen by the 800A, ACB of the source	
a	Supply Source	500kVA, 4% Z, 11kV/433V Transformer
b	OCPD as incomer at the Main LV panel	800A, ACB with fault current trip setting for an instantaneous value of 8*800A
c	Line conductor of the cable from source to Main LV Panel	20m long, 3R of 3.5 core 400 sq mm, PVC Ar Al cable
d	MET	25m long, 25*6mm Cu conductor from the Main LV panel to the MET
e	Earthing Conductor	15m long, 25*6mm Cu conductor from the MET to the neutral terminal of the supply conductor from the source
f	Neutral conductor of the cable from MET to the source winding	20m long, half core from each of the 3R of 3.5 core 400 sq mm, PVC Ar Al cable

II	Fault loop impedance seen by the 160 A, MCCB outgoing at the Main LV panel feeding LSB	
a	OCPD as outgoing at the Main LV panel	160 A, MCCB with fault current trip setting for an instantaneous value of 10*160A
b	Line conductor of the cable from the Main LV Panel up to the LSB	30m long, 3.5 C, 120 sq mm Al cable from the 160 A, MCCB outgoing at the Main LV panel up to the LSB
c	Sub MET	30m long, 25*3mm Cu conductor from the LSB to the Sub MET at the Main LV panel
III	Fault loop impedance seen by the 63A, C type MCB outgoing at the LSB feeding LDB	
a	OCPD as outgoing at the LSB	63A, C type MCB
b	Line conductor from LSB to LDB	4C, 40m long, 16 sq mm Cu cable from the 63A, C type MCB outgoing at the LSB to LDB
c	PE Conductor	45m long, 25*3mm Cu conductor from the Sub MET at the LDB to the Sub MET at the LSB
IV	Fault loop impedance seen by the 16A, C type MCB outgoing at the LDB feeding the final circuit for a socket outlet	
a	OCPD as outgoing at the LDB	16A, C type MCB
b	Line conductor from LDB to socket outlet	10m long, 4sq mm PVC class 2 cu conductor
c	PE Conductor	10m long, 4sq mm PVC class 2 cu conductor

Table 8: Data for the Fault Loop Impedance Test (Refer Fig.2)

B. CALCULATION

Table 9: Fault Loop Impedance as per design and verification

Fault Loop Impedance contributing conductors (refer Cl.6.1)	Impedance calculated from different conductors contributing fault loop, Ohms	Fault loop impedance calculated from time-current characteristics of the OCPDs (Refer Expression 1), Ohms	Maximum allowable value of fault loop impedance considering the heating effect during the fault condition. (Refer Expression 2 i.e.2/3 value of Column 3), Ohms	Measured fault loop impedance for validation from test, Ohms
1	2	3	4	5
I Fault loop impedance seen by the 800A, ACB of the source				
a. Source impedance (Refer Expression 3)	0.0150			

b. Impedance of the line conductor from the Transformer up to the 800A, ACB at the Main LV panel (3R of 3.5 core 400 sq mm PVC Al cable of 20m length) as per Table 7	0.0005			
c. Impedance of the 25m long, 25*6mm Cu conductor from the Sub MET at the Main LV panel to the MET (Refer Expression 4)	0.002873			
d. Impedance of the 15m long, 25*6mm Cu conductor from the MET to the neutral terminal of the supply conductor from the source (Refer Expression 4)	0.0017			
e. Impedance of the 20m long, half core from each of the 3R of 3.5 core 400 sq mm, PVC Ar Al cable neutral of the supply conductor up to the source winding as per Table 7	0.0011			
f. OCPD as incomer at the Main LV panel: 800A, ACB with fault current trip setting for an instantaneous value of **6400A** (Refer Expression 1)		0.0359	0.0239	
Total fault loop impedance up to the 800A Main LV panel breaker	**0.0212**			Actual test value
II Fault loop impedance seen by the 160 A, MCCB outgoing at the Main LV panel feeding LSB				
a. Impedance of phase conductor in the 30m long, 3.5 C, 120 sq mm Al cable from 160 A, MCCB outgoing at the Main LV panel up to the 125A, C Type MCB incomer at the LSB (as per Table 7)	0.0076			
b. Impedance of the 30m long, 25*3mm Cu conductor from the Sub MET at the LSB to the Sub MET at the Main LV panel (Refer Expression 4).	0.0069			
c. OCPD as outgoing at the Main LV panel: 160 A, MCCB with fault current trip setting for an instantaneous value of 1600 A (Refer Expression 1)		0.1438	0.0958	
Total fault loop impedance up to the incomer of the LDB (6444 A)	**0.0357**			Actual test value

III Fault loop impedance seen by the 63A, C type MCB outgoing at the LSB feeding LDB				
a. Impedance of the Line conductor in the 40m long, 4C, 16 sq mm Cu cable from the 63A, C type MCB outgoing at the LSB to LDB (as per Table 7).	0.0460			
b. Impedance of PE conductor 45m long, 25*3mm Cu conductor from the Sub MET at the LDB to the Sub MET at the LSB (Refer Expression 4)	0.0103			
c. OCPD as outgoing at the LDB:63A, C Type MCB (Refer Expression 1) (**630A**)		0.3651	0.2434	
Total fault loop impedance up to the LDB (**2499A**)	**0.0920**			Actual test value
IV Fault loop impedance seen by the 16A, B Type MCB outgoing at the LDB feeding socket outlet at the final circuit				
a. Impedance of the Line conductor: 10m long, 4sq mm PVC class 2 cu conductor from the LDB to the socket outlet at the final circuit (as per Table 7)	0.0461			
b. Impedance of the PE Conductor: 10m long, 4sq mm PVC class 2 cu conductor from the LDB to socket outlet at the final circuit (as per Table 7)	0.0461			
c. OCPD as outgoing at the LDB to the socket outlet at the final circuit: 16A, C type MCB (Refer Expression 1)		1.4375	0.9583	
Total fault loop impedance up to the LDB (1248A)	**0.1842**			Actual test value

A well-designed installation relies on the effectiveness of fault protection by automatic disconnection of the supply and FLIT ensures this compliance. It can be seen from the calculation that backup protection by an OCPD is also possible in case the immediate OCPD fails. e.g. The instantaneous setting of **6400A at** the 800A, ACB will override the short time delay and it can still see a fault current of **6444 A** applicable for the 160A, MCCB to ensure the required protection.

C. Testing and Reporting

Compliance is ensured by conducting a test as per cl.4.2.11.4 and Cl. 6.2.3.6.2 of Annex MM of IS 732. Test should be conducted in sequence starting from the main LV panel and ending up to the final circuit to identify the flaws at every stage for suggesting measures effectively. The test equipment should be operated as per the manufacturer's recommendations.

Details of circuit-wise OCPDs, the current causing effective operation of the OCPDs, and RCDs, calculated fault loop impedance, validation by test, and declaration of compliance or non-compliance, and the touch voltage relating to the type of earthing system should be formed in a Table (Refer Table 9). If the fault loop impedance test value is found to be lower than the calculated value, it should be reported that compliance is ensured. Otherwise, recommendation measures like replacement of oversized OCPDs, revising trip settings for the OCPDs, and enhancing the size of conductors should be reported.

- Declare as "COMPLIED" if the measured impedance (column 5 of Table 9) for validation is less than the maximum allowable impedance (column 4 of Table 9).
- Otherwise, declare as "NOT COMPLIED".

The 2/3 of the calculated value of loop impedance (column 2 in Table 6) should be taken as a reference to suggest suitable measures for compliance. Possible measures are:

i) Identifying ineffectiveness in the TNS system at every stage, (e.g. avoidance of direct connection between the source earthing lead and MET can affect the whole installation from compliance).
ii) improving the design by enhancing the sizing among the fault loop forming conductors with reference to the calculated impedance;
iii) selection of suitable OCPDs and/or revising trip settings with reference to the time-current characteristics of the manufacturer's data;
iv) reducing the contact resistance of conductors forming the fault loop impedance path;
v) Reducing the oversized OCPDs by lower-rated ones and effective TNS at the upstream source will help to achieve the desired fault loop impedance value. There are wrong installation practices, say, not providing TNS earthing system on the secondary side of the isolation transformer.

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